WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of functional circuit blocks for performing predetermined processing based on the number of clocks when an instruction or data is inputted thereto,

each of said plurality of functional circuit blocks comprising:

a power status control circuit for controlling a power status of each of said plurality of functional circuit blocks; and

a prediction circuit for controlling said power status control circuit in accordance with the instruction or the data which is inputted thereto.

2. A device according to Claim 1, wherein said prediction circuit has a function for controlling the processing for inputting the instruction or the data to each of said plurality of function circuit blocks.

3. A device according to Claim 1, wherein when there is no said input to said plurality of functional circuit blocks until the number n of clocks, said power status control circuit comprises at least one of a power shutdown circuit for shutting down power, an operating voltage setting circuit for setting an operating voltage to be low, and an operating frequency setting circuit for setting an operating frequency to be low.

4. A device according to Claim 1, wherein said power status control circuit which is connected between a power supply for supplying power to each of said plurality of functional circuit blocks and each of said plurality of functional circuit blocks, comprises a power shutdown circuit for shutting down power which is supplied to each of said plurality of functional circuit blocks,

said prediction circuit comprises a counter for counting the number of clocks inputted to each of said plurality of functional circuit blocks and outputting, when the number of clocks is n, a signal thereof, control means for controlling said power shutdown circuit, and an input detection circuit for detecting the input, outputting, when there is no input, a signal thereof to said control means, and outputting a reset signal for resetting said counting, and

said control means performs AND operation of outputs of said counter and said input detection circuit and controls said power shutdown circuit.

5. A device according to Claim 4, wherein said functional circuit block comprises a register for temporarily storing said input and a functional block for computation, and

said prediction circuit further comprises a comparator for controlling said register by comparing the output of said control means with the number of clocks.

6. A device according to Claim 1, wherein said power status control circuit which is connected between a power supply for supplying power to each of said plurality of functional circuit blocks and each of said plurality of functional circuit block, comprises an operating voltage setting circuit for setting an operating voltage of each of said plurality of functional circuit blocks by a signal voltage which is applied to said power status control circuit,

said prediction circuit comprises a switch control circuit for controlling a switch provided between a plurality of control signal lines which apples different voltages and said operating voltage setting circuit, by determining when and which one of said control signal lines is connected to said operating voltage setting circuit based on the input to said plurality of functional circuit blocks and said number of clocks, and

said switch control circuit controls an operation for connecting one of said control signal lines, which applies the highest voltage, to said operating voltage setting circuit, when the data or the instruction is inputted to each of said plurality of functional circuit blocks, and also controls an operation for determining which one of said control signal lines, which applies the lowest voltage, is connected to said operating voltage setting circuit, when the number of the clocks reaches n after the data or the instruction is inputted to each of said plurality of

functional circuit blocks.

7. A device according to Claim 6, wherein each of said plurality of functional circuit blocks comprises a register for temporarily storing the input and a functional block for computation, and

said switch control circuit further comprises a function for controlling said register in accordance with the input and the number of clocks.

8. A device according to Claim 1, wherein said power status control circuit, comprises an operating frequency setting circuit for setting an operating frequency of each of said plurality of functional circuit blocks to be low, having a frequency divider for varying a frequency dividing ratio,

said prediction circuit comprises: an input detection/clock counting circuit for detecting the instruction or data which is inputted to each of said plurality of functional circuit blocks, counting the number of clocks, and controlling said frequency divider; and a setting register for, when the number of clocks reaches n after the instruction or the data is not inputted to each of said plurality of functional circuit blocks, setting the number n of clocks so as to control power so that it becomes low and for storing said number n of clocks, and,

when the counted number of clocks is n that is stored in said setting register after the instruction or the data

is not inputted to each of said plurality of functional circuit blocks, said input detection/clock counting circuit controls a frequency of the clock which is inputted to each of said plurality of functional circuit blocks by increasing the frequency dividing ratio of said frequency divider.

9. A device according to Claim 8, wherein each of said plurality of functional circuit blocks comprises a register for temporarily storing the input and a functional block for computation, and

said input detection/clock counting circuit further has a function for controlling said register in accordance with said input and the number of clocks.

10. A device according to Claim 3, further comprising a circuit for updating said number n of clocks in accordance with a history.

11. A device according to Claim 10, further comprising a rewritable nonvolatile semiconductor memory for storing an update result.

12. A device according to Claim 1, further comprising a CPU comprising a power control table corresponding to said plurality of functional circuit blocks, said CPU outputting a control signal for controlling said power status control circuit by referring to said power control table and said instruction or data which is inputted to each of said

functional circuit blocks.

13. A device according to Claim 12, wherein said CPU further comprises a decoder for decoding power controlling information of said plurality of functional circuit blocks, including the instruction or the data which is externally inputted to said CPU, so as to obtain said control signal for controlling said power status control circuit connected to each of said plurality of functional circuit blocks.

14. A device according to Claim 13, wherein said CPU totally controls power of said plurality of functional circuit blocks based on said control signal which is obtained by the decoding of said power controlling information by using said decoder, and said CPU does not control each of said plurality of functional circuit blocks.